

# SPECIFICATIONS FOR THE NI PXI/PCI-5411/5431

## NI PXI/PCI-5411 High-Speed Arbitrary Waveform Generator

## NI PXI/PCI-5431 Video Waveform Generator

This document lists the specifications for the NI PXI/PCI-5411 and the NI PXI/PCI-5431. These specifications are typical at 25 °C unless otherwise stated. The operating temperature range is 0–50 °C.

### Analog Output

Number of channels ..... 1

Resolution ..... 12 bits

Maximum update rate ..... 40 MHz

DDS accumulator ..... 32 bits

Frequency range

Waveform Type	NI PXI-5411	NI PXI-5431
Arb	40 MS/s	40 MS/s
PAL-B, STANDARD PAL, N-PAL, Combination N-PAL, SECAM	—	40 MS/s
NTSC/PAL-M	—	40.02797 MS/s
PAL-M	—	40.009739 MS/s
SYNC (TTL)	16 MHz, max	8 MHz, max
Square	1 MHz, max	1 MHz, max
Ramp	1 MHz, max	1 MHz, max
Triangle	1 MHz, max	1 MHz, max

Frequency resolution (DDS mode) ..... 9.31 MHz

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## Voltage Output

Ranges .....	$\pm 5$ V into a 50 $\Omega$ load; $\pm 10$ V into a high-impedance load
Accuracy .....	$\pm 0.1$ dB
Output attenuation .....	0 to 73 dB
Resolution .....	0.001 dB steps
Pre-attenuation offset	
Range .....	$\pm 2.5$ V into 50 $\Omega$ <sup>1</sup>
Accuracy .....	$\pm 5$ mV
Output coupling .....	DC
Output impedance .....	50 $\Omega$ or 75 $\Omega$ , software selectable
Load impedance .....	50 $\Omega$ or greater
Output enable .....	Software switchable
Protection .....	Short-circuit protected
Typical rise/fall time .....	8 ns (10–90% 0–5 V square wave into 50 $\Omega$ load, filters off)

## Sine Spectral Purity

Harmonic products and spurs	
Up to 1 MHz .....	–60 dBc
Up to 16 MHz .....	–35 dBc
Phase noise .....	–105 dBc/Hz at 10 kHz from carrier

## Filter Characteristics

Digital	
Type .....	Half-band interpolating
Selection .....	Software switchable (enable or disable)
Taps .....	67
Filter coefficients .....	Fixed 20-bit

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<sup>1</sup> With less than 10 dB of attenuation, signal maximum plus offset (before attenuation) must not exceed  $\pm 5$  V (into 50  $\Omega$ ).

Data interpolating frequency ..... 80 MS/s  
Pipeline signal delay ..... 26 sampling periods

#### Analog

Type ..... 7th-order L-C lowpass filter  
Passband ripple .....  $\pm 2$  dB

## Waveform Specifications

#### Memory

##### Arb mode

NI 5411 ..... 2,000,000 16-bit samples

NI 5431 ..... 8,000,000 16-bit samples

DDS mode..... 16,384 16-bit samples

#### Segment length

Arb mode ..... 256 samples, minimum,  
multiples of 8 samples

DDS mode..... 16,384 samples, exact

Max segments in waveform memory ..... 5,000 (Arb mode only)

#### Segment linking (instruction FIFO)

Arb mode ..... 292 links

DDS mode..... 512 links

#### Segment looping (Arb mode only)

Count..... 65,536 loops

## Timing I/O

Update clock ..... Internal, 40 MHz, max

Interval count ..... 2–65,535

#### Phase locking

External reference sources ..... Input connector, RTSI clock line,  
or internal

Reference clock frequencies ..... 1 MHz, 5–20 MHz in 1 MHz steps

#### Frequency locking range

NI 5411 .....  $\pm 100$  ppm

NI 5431 .....  $\pm 500$  ppm

# Triggers

## Digital Trigger

Compatibility .....	TTL
Response .....	Rising edge
Pulse width ( $T_{d1}$ ).....	20 ns, minimum
Trigger to waveform output (Arb mode) delay ( $T_{d2}$ ) .....	76 sample clocks plus 38 ns, max
Trigger to waveform output (DDS mode) delay ( $T_{d2}$ ) .....	28 sample clocks plus 150 ns, max

## RTSI

Trigger lines.....	7
Clock lines .....	1

## Bus Interface

Type .....	Slave
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## Operational Modes

Type .....	Single, continuous, burst, stepped
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## Other Outputs

### SYNC Out

Level .....	TTL
Duty cycle.....	20–80%, software controllable

### Marker Output

Types .....	TTL
Location .....	User defined, one per stage
Pulse width ( $T_{d4}$ ).....	8 sample clock periods
Arb output delay from marker ( $T_{d3}$ ) .....	50 ns, max

## Digital Pattern Output

Sample rate..... 40 MHz, max  
 Resolution ..... 16 bits  
 Sample clock logic ..... TTL  
 Clock pulse HIGH time..... 25 ns fixed  
 (for clock interval counts > 1)

PCLK to pattern data  
 output time ( $T_{co}$ )..... 1 ns, max

Digital pattern logic ..... TTL

Logic level output ratings for SYNC, marker, digital pattern,  
 and sample clock outputs

Type	Min	Max
$V_{OH}$	3.0 V	—
$V_{OL}$	—	0.7 V
$I_{OH}$	—	1.0 mA
$I_{OL}$	—	1.0 mA

$V_{OH}$  = voltage output for logic level 1  
 $V_{OL}$  = voltage output for logic level 0  
 $I_{OH}$  = current output for logic level 1  
 $I_{OL}$  = current output for logic level 0

## External PLL Reference Input

Frequency..... 1 MHz or 5–20 MHz in  
 1 MHz steps

Amplitude.....  $1 V_{pk-pk} \leq \text{level} \leq 5 V_{pk-pk}$

## Internal Clock

Frequency..... 40 MHz

Initial accuracy.....  $\pm 5$  ppm

Temperature stability (0 to 50 °C).....  $\pm 25$  ppm

Aging (1 year).....  $\pm 5$  ppm

## External Clock Reference Input

Frequency .....	40 MHz, max
Amplitude .....	TTL

## Mechanical

### Connectors

ARB/Video (output) .....	SMB/BNC
SYNC (output).....	SMB/BNC
PLL reference (input) .....	SMB
Digital I/O (digital pattern out, marker out, external trigger in).....	50-pin digital, SMB (for PXI)

Size ..... 1 slot

Power requirements ..... 5 V, 3.5 A, max;  
12 V, 125 mA

## Safety

Designed in accordance with IEC 61010-1, EN 61010-1, UL 3111-1, and CAN/CSA C22.2 No. 1010.1 for electrical measuring and test equipment.

## Electromagnetic Compatibility

EMC/EMI ..... CE, C-Tick, and FCC Part 15  
(Class A) Compliant

Electrical emissions ..... EN 55011 Class A at 10 m  
FCC Part 15A above 1 GHz

Electrical immunity ..... Evaluated to EN 61326-1:1997  
A1:1998, Table 1



**Note** For full EMC and EMI compliance, you must operate this device with shielded cabling. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity** at [ni.com/hardref.nsf/](http://ni.com/hardref.nsf/). This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC (in Adobe Acrobat format) appears. Click the Acrobat icon to download or read the DoC.